Claims

What is claimed is:

1. A step-down circuit, comprising:

a clock control circuit which provides a plurality of clock signals having a frequency determined based on a control signal;

a charge pump circuit which reduces a first potential applied to a first terminal so as to provide a second potential from a second terminal by switching a connection of a plurality of capacitors in sync with the plurality of clock signals output from the clock control circuit; and

a comparator which produces the control signal supplied to the clock control circuit by comparing the second potential to a reference potential.

2. The step-down circuit according to Claim 1, further comprising:

a circuit which generates the reference potential based on the first potential applied to the first terminal of the charge pump circuit.

3. The step-down circuit according to Claim 1, the clock control circuit, comprising:

a frequency divider which divides an input clock signal;

a selection circuit which selects one of the input clock signal and a clock signal divided by the frequency divider, based on the control signal provided by the comparator; and

an output circuit which provides the plurality of clock signals to be provided to the charge pump circuit based on the one clock signal selected by the selection circuit.

4. A power supply circuit providing a plurality of potentials from a plurality of terminals based on a first potential, comprising:

a voltage divider which divides the first potential;

a voltage follower which provides a second potential based on the first potential divided by the voltage divider; and

a step-down circuit which reduces at least one of the first potential and the second potential so as to provide a third potential by switching a connection of a plurality of capacitors in sync with a clock signal.

5. The power supply circuit according to Claim 4, further comprising:

a booster which increases the first potential so as to provide a fourth potential;

a second voltage divider which divides the fourth potential;

a second voltage follower which provides a fifth potential based on the divided fourth potential; and

a second step-down circuit which reduces at least one of the fourth potential and the fifth potential so as to provide a sixth potential, by switching a connection of a second plurality of capacitors in sync with a clock signal.

6. The power supply circuit according to Claim 4, further comprising:

a stabilized power supply circuit which produces a stabilized power

supply potential; and

an operational amplifier which produces the first potential by amplifying the stabilized power supply potential produced by the stabilized power supply circuit with a predetermined amplification factor.

7. A semiconductor integrated circuit, comprising:

the step-down circuit according to Claim 1.

8. A semiconductor integrated circuit, comprising:

the power supply circuit according to Claim 4.

9. The step-down circuit according to Claim 2, the clock control circuit, comprising:

a frequency divider which divides an input clock signal;

a selection circuit which selects one of the input clock signal and a clock signal divided by the frequency divider, based on the control signal provided by the comparator; and

an output circuit which provides the plurality of clock signals to be provided to the charge pump circuit based on the one clock signal selected by the selection circuit.

10. The power supply circuit according to Claim 5, further comprising:

a stabilized power supply circuit which produces a stabilized power supply potential; and

an operational amplifier which produces the first potential by amplifying the stabilized power supply potential produced by the stabilized power supply circuit with a predetermined amplification factor.